AMENDMENTS TO THE CLAIMS:

This listing of claims replaces all previous versions and listing of claims in the subject application:

Listing of Claims:

1. (Currently Amended) A computer processor for processing (i) instruction packets comprising a plurality of only control instructions, the control instructions having a control bit width, and (ii) instruction packets comprising a plurality of instructions comprising at least one data processing instruction, the data processing instructions having a data processing bit width wider than the control bit width, the processor comprising:

a decode unit for decoding sequentially the instruction packets fetched from a memory holding the instruction packets;

a control processing channel capable of performing control operations, the control processing channel comprising a plurality of functional units including a control register file having a first bit width; and

a data processing channel capable of performing data processing operations at least one input of which is a vector, the data processing channel comprising a plurality of functional units including a data register file having a second bit width, wider than the first bit width;

wherein the decode unit comprises decode circuitry configured to decode identification bits of each instruction packet to determine which type (i), (ii), of instruction packet is being decoded, and control circuitry configured to pass the plurality of only control instructions from an instruction packet of type (i) to the control processing channel when the decode circuitry indicates so and to pass the plurality of instructions comprising at least one data processing instruction from an instruction packet of type (ii) to the data processing channel when the decode circuitry indicates so;

wherein, in use the decode unit causes instructions of (i) instruction packets comprising a plurality of only control instructions to be executed sequentially on the control processing channel; and

wherein, in use the decode unit causes instructions of (ii) instruction packets comprising a plurality of instructions comprising at least one data processing instruction to be executed simultaneously on the data processing channel.

2. (Previously Presented) A computer processor according to claim 1, wherein the control processing channel further comprises a branch unit and a control execution unit.

3. (Previously Presented) A computer processor according to claim 1, wherein the data processing channel further comprises a fixed data execution unit and a configurable data execution unit.

4. (Original) A computer processor according to claim 3, wherein the fixed data execution unit and the configurable data execution unit both operate according to a single instruction multiple data format.

5. (Previously Presented) A computer processor according to claim 1, wherein the control and data processing channels share a load store unit.

6. (Previously Presented) A computer processor according to claim 5, wherein the load store unit uses control information supplied by the control processing channel and data supplied by the data processing channel.

7. (Original) A computer processor according to claim 1, wherein the instruction packets are all of equal bit length.

8. (Original) A computer processor according to claim 7, wherein the instruction packets are all of a 64-bit length.

9. (Original) A computer processor according to claim 1, wherein the control instructions are all of a bit length between 18 and 24 bits.

10. (Original) A computer processor according to claim 9, wherein the control instructions are all of a 21-bit length.

11. (Original) A computer processor according to claim 7, wherein the nature of each instruction in an instruction packet is selected at least from a control instruction, a data instruction, and a memory access instruction.

12. (Original) A computer processor according to claim 11, wherein the bit length of each data instruction is 34 bits.

13. (Original) A computer processor according to claim 11, wherein the bit length of each memory access instruction is 28 bits.

14. (Previously Presented) A computer processor according to claim 1, wherein when the decode unit detects that the instruction packet defines three control instructions, the decode unit is operable to supply the control processing channel with the three control instructions whereby the three control instructions are executed sequentially.

15. (Previously Presented) A computer processor according to claim 1, wherein when the decode unit detects that the instruction packet defines two instructions comprising at least one data instruction, the decode unit is operable to supply the data processing channel with at least the data instruction whereby the two instructions are executed simultaneously.

16. (Previously Presented) A computer processor according to claim 1, wherein the decode unit is operable to read the values of a set of designated bits at predetermined bit locations in each instruction packet of the sequence, to determine:

a) whether the instruction packet defines a plurality of control instructions or a plurality of instructions of which at least one is a data instruction; and

b) where the instruction packet defines a plurality of instructions of which at least one is a data instruction, the nature of each of the two instructions selected from: a control instruction; a data

instruction; and a memory access instruction.

17. (Original) A computer processor according to claim 3, wherein the configurable data execution unit is capable of executing more than two consecutive operations on the data provided by a single issued instruction before returning a result to a destination register file.

18. (Currently Amended) A method of operating a computer processor for processing (i) instruction packets comprising a plurality of only control instructions, the control instructions having a control bit width, and (ii) instruction packets comprising a plurality of instructions comprising at least one data processing instruction, the data processing instructions having a data processing bit width wider than the control bit width, the processor comprising a decode unit for decoding sequentially the instruction packets fetched from a memory holding the instruction packets; a control processing channels comprising a plurality of functional units including a control register file having a first bit width; and a data processing channel capable of performing data processing operations at least one input of which is a vector, the data processing channel comprising a plurality of functional units including a data register file having a second bit width, wider than the first bit width, the method comprising:

decoding identification bits of each instruction packet to determine which type (i), (ii), of instruction packet is being decoded, and passing the plurality of only control instructions from an instruction packet of type (i) to the control processing channel when the decode circuitry indicates so and passing the plurality of instructions comprising at least one data processing instruction from an instruction packet of type (ii) to the data processing channel when the decode circuitry indicate so;

when the instruction packet defines (i) a plurality of only control instructions supplying the control instructions to the control processing channel wherein the control instructions are executed sequentially; and

when the instruction packet defines (ii) a plurality of instructions comprising at least one data processing instruction, supplying at least the data instruction to the data processing channel wherein

the plurality of instructions are executed simultaneously.

19.-20. (Canceled)

21. (Currently Amended) A computer program product comprising program code means which include a sequence of instruction packets,

said instruction packets including a first type of instruction packet comprising a plurality of only control instructions of ~~substantially~~ equal ~~length~~ width , the control instructions having a control bit width, and a second type of instruction packet comprising a plurality of instructions comprising at least one data processing instruction, the at least one data processing instructions having a data processing bit width wider than the control bit width, and wherein at least one data processing instruction is a vector,

said instruction packets including at least one indicator bit at a designated bit location within the instruction packet, wherein the computer program product is adapted to run on a computer such that said indication bit is adapted to cooperate with a decode unit of the computer to designate whether:

a) the instruction packet defines a plurality of only control instructions or a plurality of instructions comprising at least one data processing instruction; and

b) in the case when there is a plurality of instructions comprising at least one data instruction, the nature of each of the first and second instructions selected from: a control instruction; a data instruction; and a memory access instruction.